USN

First / Second Semester B.E. Degree Examination, June/July 2011

Basic Electronics

Time: 3 hrs. Max. Mark						
No	;	: 1. Answer any FIVE full questions, choosing at least two from each 2. Answer all objective type questions only in OMR sheet page 5 of t. 3. Answer to objective type questions on sheets other than OMR will	he answer booklet.			
		PART – A				
1	a.	 Choose the correct answers for the following: i) Forward voltage across a conducting silicon diode is 				
		A) 0.3V B) 0.7V C) -0.7V ii) Zener diode regulates only when it is connected in mode.	D) -0.3V			
		A) forward bias B) reverse bias C) short	D) open			
		iii) I_{rms} for half wave rectifier is A) $\frac{I_m}{2}$ B) $\frac{I_m}{\sqrt{2}}$ C) $\frac{2 I_m}{\pi}$	D) I _m			
		$\chi_{\mathcal{L}}$ π	D) $\frac{l_m}{\pi}$			
		iv) Peak inverse voltage for bridge rectifier is A) V_m B) $2V_m$ C) $\frac{V_m}{2}$	V (04 Marrian)			
	K	L	D) $\frac{V_m}{\sqrt{2}}$ (04 Marks)			
	U.	Deduce the following for FWR: i) I _{rms} ii) I _{dc} iii) Ripple factor iv) Efficiency of rectific	cation. (08 Marks)			
	c.	 i) Calculate the ripple voltage of a full wave rectifier with a 120 μf cap a load and load current of 60 mA, frequency of 50 Hz. ii) If the peak voltage of the rectified wave is 60V, calculate the DC voltage. 				
		iii) Calculate the ripple factor.	(08 Marks)			
2	a.	Choose the correct answers for the following: i) When a transistor is used as a switch, it works in the following reg	rion :			
		A) active and cut-off B) saturation and cut				
		C) saturation and active D) none of these ii) If the transistor amplifier has voltage gain of 100, if the input voltage is 15 mV, t the output voltage is				
`		A) 1.5V B) 15V C) 0.15V	D) 1.15V			
		iii) The phase difference between input and output of an emitter follow A) in-phase B) out-of-phase C) 90° iv) An amplifier is generally connected in mode.	wer is D) 45°			
	D) short (04 Marks)					
	b.	A) saturation B) cut-off C) active A transistor amplifier connected in CE mode has $\beta = 100$ and $I_B = 5$ values of I_C , I_E and α .	60 μA. Compute the			
	c .		(06 Marks) duce the relationship (10 Marks)			

3	a.	Cho	ose the correct answer	s for the followi	ng:			
		i)	Which is the bias tec	hnique that is ve	ry widely used			
		•	A) fixed	B) collector	C) emitter	D) voltage divid	er	
		ii)	Which transistor bias	circuit has poo	r stability because its Q-p	oint varies with β_{dc} ?		
16		,	A) collector feedback		B) base			
			C) voltage divide		D) emitter			
		iii)	Emitter follower is a					
		111)	A) voltage amplifier		B) current amplif	ier		
			· · · · · ·		D) none of these			
			C) attenuator	on input of 1 vo	olt, then its output voltage	is		
		iv)		an input of 1 vo	C) 1V	D) 5V (04 Mai	rks)	
			A) 0.5V	B) 10V			-	
	b.	Expl	ain the concept of vol	age divider blas	technique using transisto	$2.2VO \text{ and } V_{} = 1$		
	C.	A collector to base circuit has $V_u = 24V$, $R_B = 180K\Omega$, $R_C = 3.3K\Omega$ and $V_{CE} = 10V$.						
		Calculate h_{FE} , determine V_{CE} when a new transistor is replaced having $h_{FE} = 120$. (66 Marks)						
4	a.	Cho	ose the correct answer	s for the follow	ng:		* 4	
		i)	The function of gate	in SCR is to con	ntrol the			
			A) flow of current		B) voltage regula	ition	1.	
11		7	C) voltage amplifica	tion	D) none of these			
		ii)	n of UJT is known a					
		11)	A) ON		B) pulse			
			C) negative		D) intrinsic stand	i-off		
		1115	The minimum noint	in V.I character	istic of UJT is known as			
		iii)		B) valley	C) latching	D) firing		
			A) negative	D) valley				
		iv)			ch I _D becomes essentially B) cut-off voltag	A COMPUNITION		
			A) pinch-off voltage				rke)	
			C) breakdown voltage		D) ohmic voltage	(04 Ma		
	b.	Exp	lain V-I characteristic	of SCR.				
	C.	Exp	lain working principle	of UJT.		(08 Ma	II N3)	
				PAR	T-B			
5	a.	Cho	ose the correct answe	rs for the follow	ring:			
3	ш.	i)	Cut-off frequencies	of an amplifier	are also called as			
		1.)	A) half power points		B) square points	,		
			C) amplified points		D) none of these			
		:::\	The objective of usi	na a crystal osci				
		ii)		ing a crysum oso	B) 50-70 Hz			
			A) DC		D) variable frequency	nencv		
			C) stable frequency		D) variable nod	2020)		
		iii)	An oscillator uses	•	B) +ve feedback			
			A) negative feedbac		•			
			C) +ve and -ve fee	iback	D) none of these			
		iv)	Which of the follow	ving oscillators i	s used to generate high fro	equencies?		
		-	A) RC-phase shift		B) wien bride			
	٠.		C) L-C oscillator		D) blocking osc			
	b.	Ext	plain the working of R	C coupled ampl	ifier with its frequency res		arks)	
	C.	Ext	olain Barkhauson crite	rion.		(02 M		
		In a	Hartley oscillator I.	$= 20 \mu H I_0 = 2$	2 mH and capacitor is var	iable. Find the range	of C	
	d.	ice m g	name of the started from	n 1 MHz to 2 5	MH ₂	(06 M	arks)	

6	a.	Choose the correct answers for the following:			
		i) An ideal OP-AMP has			
		A) infinite input impedance	B) infinite voltage g	gain	
		C) zero output resistance	D) all of these		
		ii) The differential amplifier has			
		A) one input and one output	B) two inputs and to	wo outputs	
			D) one input and tw	o outputs	
		iii) An OP-AMP shorted between inverting te		-	ed
			C) integrator		
		iv) The voltage gain of an OP-AMP in the or			
		A) 10^1 B) 10^2	C) 10 ⁴	D) 10^6	(04 Marks)
	h	Draw the following circuits using OP-AMP:	- /	-,	
		i) adder ii) voltage follower iii) integ	rator iv) different	tiator	(08 Marks)
	c.				(08 Marks)
	Ο.	Explain the working or extr.			(00 1.1)
7	a.	Choose the correct answers for the following:			
,	a.	i) The two complement of (1 0 0 1) ₂ is			
		A) 1001 B) 0010	C) 0110	D) 1010	
		ii) The decimal number 20 in hexadecimal co		2) 1010	
		A) 41 B) 14	C) 140	D) 410	
				<i>D)</i> 110	•
			C) amplification	D) atten	nation
			C) ampinication	D) accon	uation
		iv) 9's complementation is used for	C) multiplication	D) divis	ion
		A) addition B) subtraction	C) multiplication	D) aivis	(04 Marks)
	L	Explain the working of super heterodyne receive	er with a suitable block	diagram	
			diagram.	(00 1/12/12)	
	C.				
		i) $(1010101111100)_2 = (?)_8 = (?)_{16}$			
		ii) $(240)_{10} = (?)_2 = (?)_{BCD}$	44		
		iii) $(28)_{10} - (19)_{10}$ using 1's and 2's complement	ent metnod		(00 351)
		iv) $(1100)_2 + (1111)_2$ and $(123)_8 + (126)_8$			(08 Marks)
8	a.	Choose the correct answers for the following:	4		
		i) Simplified form of Boolean expression of			_
		A) 1 B) AB	C) AB	D) A + 1	В
		ii) Expression for EX-OR gate with inputs 'A	'and 'B' is		
		A) $A + B$ B) $A\overline{B} + \overline{B}A$	C) $AB + \overline{A}\overline{B}$	D) none	of these
			•	,	
		iii) Simplification of AB is			=
		$A) A + B \qquad B) A + B$	C) A+B	D) \overline{A} +	В
		iv) Full adder has inputs.			
		A) 1 B) 2	C) 3	D) 4	(04 Marks)
	b.	i) Realize $Y = \overline{AB} + A\overline{B}$ by using minimum n	umber of NAND gates	•	
		ii) Simplify ABC+ABC+ABC+ABC and re			(08 Marks)
	C.	State and prove Demorgan's theorem.			(04 Marks)
	đ.	Simplify $\overline{\overline{XY} + \overline{XYZ}} + X(Y + X\overline{Y})$.			(04 Marks)
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3 of 3

(07 Marks)

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First/Second Semester B.E. Degree Examination, June/July 2011 **Basic Electronics**

Ti	me:	: 3 hrs.	Max. Marks:100
No	1	I.Answer FIVE full questions choosing at lo 2.Answer all objective type questions only in 3.Answers to objective type questions on she	OMR sheet page 5 of the Answer Booklet.
		PART -	- A
1	a.	i) An excessively high reverse voltage ap known as:	oplied to a junction diode will cause an effect
		A) punch through B) saturation	C) diffusion D) avalanche break down
		ii) Forward biasing a P-N junctionA) increases its resistanceC) shorts the junction	B) decreases its resistance D) increases the potential barrier height
		iii) When a diode is heavily doped,A) the zener voltage will be lowC) the depletion region will be thin	B) the avalanche voltage will be high D) the leakage current will be low.
		iv) Leakage current of a junction diodeA) is due to majority carriersC) is in mA or μA range	B) decreases with temperature D) depends on the method of its fabrication.
	b.	What is a P-N junction? Discuss its behaiii) Reverse bias.	(04 Marks) aviour under i) No bias; ii) Forward bias; (10 Marks)
	c.	For a bridge rectifier circuit, derive the exefficiency.	· · · · · · · · · · · · · · · · · · ·
2	a.	Select the correct answer: i) The efficiency of half wave rectifier is A) 40.6% B) 0.46% (C) 1.21% D) 81.2%
		ii) A zener diodeA) is always forward biasedC) has a sharp breakdown at low reverse v	B) is connected in series
		iii) A filter circuit is used to remove the	C) Both A and B D) None of these.
		burn out and hence short diodes.	fier is connected across the dc terminals, it will
	•	-	three D) four (04 Marks)
	b.	resistance of each diode is 25Ω and the load re-	i) efficiency of rectification iv) PIV across
	c.	•	(09 Marks) at gain characteristics. Explain the shape of the

Select the correct answer: 3

i) The biasing circuit, which gives most stable operating point is

B) Collector to base bias C) Voltage divider bias D) None of these

ii) The arrow on the emitter of a transistor indicates

A) the direction of electron flow

B) the positive voltage point

C) the direction of positive current flow D) the ground connections.

iii) The common emitter transistor circuit configuration is most often used because of its higher

A) power gain

B) frequency

C) output impedance

D) voltage gain.

iv) In a transistor with normal bias, the emitter junction

A) is reversed biased

B) has a high resistance

C) has a low resistance

D) emits carriers in base which are in majority there

(04 Marks)

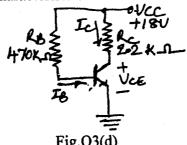
b. Define '\alpha' and '\beta' of a transistor. Show that $\beta = \frac{\alpha}{(1-\alpha)}$.

(04 Marks)

c. Discuss the causes of unstability in a transistor.

(06 Marks)

d. In the circuit shown in Fig.Q3(d), a NPN Transistor with $\beta = 100$ is used. Find I_C and V_{CE}. Draw the DC load line output characteristics and indicate the Q point. Take $V_{BE} = 0.7$ Volts.



(06 Marks)

Select the correct answer:

i) A JFET behaves like a

A) Resistor

B) Constant current

C) Constant voltage source

D) All the above in different regions.

ii) When JFET is operated above pinch off voltage, its drain current

A) increases sharply

B) becomes constant

C) starts decreasing

D) becomes zero.

iii) The output of a UJT can be taken from its

A) base 1

B) base 2

C) emitter

D) any one of three terminals

iv) When a UJT is turned ON, the resistance between emitter terminal and base 1 is

A) increased

B) decreased

C) zero

D) infinite

b. Sketch the voltampere characteristic of a typical silicon-controlled rectifier. Explain the behavior of the SCR reference to its V-I characteristic. (08 Marks)

c. Draw the output characteristics of a P-channel JFET with external bias. Indicate various (08 Marks) regions of operation and explain the shapes of the curves qualitatively.

PART - B

5	i) As compared to the resistance of the source, the input impedance of a good			
		amplifier should be A) high B) low C) equal D) twice.		
		 ii) Coupling capacitors mainly affect A) upper cut-off frequency C) with upper and lower cutoff frequency D) gain in high frequency range. 		
		 iii) The voltage gain of a common-base amplifier depends upon A) load resistor RL B) Input resistance of transistor C) ac alpha D) All the above. 		
		iv) In a common base amplifier, a smaller load resistance will produce: A) high voltage gain B) high current gain C) low power gain D) all the above. (04 Marks)		
	b.	What is an oscillator? Write the circuit of a phase-shift oscillator and describe its operation given the expression for its frequency of oscillation. (09 Marks)		
	c.	Sketch a typical frequency response graph for an RC coupled amplifier. Briefly explain the salient points on it. (07 Marks)		
6	a.	Select the correct answer: i) An advantage of an inverting amplifier is its ability to handle input at a time. A) more than one B) less than one C) equal to one D) None of these.		
		ii) Op-amp is a direct coupled multistage A) voltage amplifier B) current amplifier C) voltage-current amplifier D) power amplifier		
		iii) The common-mode rejection ratio of an ideal op-amp is A) zero B) low C) high D) infinite.		
		iv) converts physical quantity to electrical signal. A) Receiver B) Transducer C) Modulator D) Transmitter. (04 Marks)		
	b.	Derive an expression for output voltage of an op-amp i) Inverting amplifier ii) Adder iii) Integrator. (10 Marks)		
	c.	will a large way by the term modulation? Why is it required in communication system?		
7	a.	Select the correct answer: i) Radio communication is the process of sending information in the form of A) mechanical signal B) electrical signal C) electro-mechanical signal D) all of these.		
		ii) $(762)_8 = (?)_{10}$ A) $(468)_{10}$ B) $(248)_{10}$ C) $(128)_{10}$ D) $(498)_{10}$		
		iii) $(0.125)_{10} = (?)_2$ A) $(0.001)_2$ B) $(0.010)_2$ C) $(0.100)_2$ D) $(0.110)_2$		
		iv) Computer system only support numbers for the A) binary data B) decimal number C) hexadecimal number D) octal number (04 Marks)		

		ii) $(44030)_{10} = (?)_{16}$ iii) $(44030)_{10} = (?)_{2} = (?)_{16}$ iii) To subtract $(101011)_2$ from $(100110)_2$ using 2's comp	olement. (09 Marks)
	c.	c. A 500 W, 1 MHz carrier is amplitude modulated with a sinusoida depth of modulation is 60%. Calculate the band width power in the power transmitted.	signal of 1 kHz The
	d.	d. Write the symbol, truth table and output expression for EX-OR gate.	(03 Marks)
8	a.	 a. Select the correct answer: i) In a half adder when both the inputs A and B are high then A) SUM = 1 and carry = 0 B) SUM = 0 and carry = 0 C) SUM = 0 and carry = 1 D) All of these. 	
		ii) NAND gate is a combination of gate. A) OR and NOR B) NOT and NAND C) NOT and AND D) None of these.	
•		iii) Demorgan theorem states that $\overline{A + B} = $ A) $\overline{A} + \overline{B}$ B) $\overline{A} \cdot \overline{B}$ C) \overline{AB} D) None of iv) $A + \overline{A} = $ A) 0 B) 1 C) A D) None of	•
	b.		
	c.	c. Draw the circuit of a TWO input transistor logic NAND gate. Explain	(06 Marks) its operation. (07 Marks)
	d.	d. Draw the logic circuit of Full adder.	(03 Marks)